ANALOG DEVICES

Simultaneous Sampling Dual 200 ksps 14-Bit ADCs

Preliminary Technical Data

AD7863

FEATURES

Two Fast 14-Bit ADCs
Four Input Channels
Simultaneous Sampling & Conversion
4.5µs Conversion Time
Single Supply Operation
Selection of Input Ranges:
  ±10 V for AD7863-10
  ±2.5 V for AD7863-3
  0 to 2.5 V for AD7863-2
High Speed Parallel Interface
Low Power, 75mW typ
Power Saving Mode, 50uW typ
Overvoltage Protection on Analog Inputs
14 Bit pin compatible upgrade to AD7862

APPLICATIONS

AC Motor Control
Uninterrupted Power Supplies
Data Acquisition Systems
Communications

GENERAL DESCRIPTION

The AD7863 is a high speed, low power, dual 14-Bit A/D converter that operates from a single +5 V supply. The part contains two 4.5 µs successive approximation ADCs, two track/hold amplifiers, an internal +2.5 V reference and a high speed parallel interface. There are 4 analog inputs which are grouped into two channels (A & B) selected by the A0 input. Each channel has two inputs (V_{A1} & V_{A2} or V_{B1} & V_{B2}) which can be sampled and converted simultaneously thus preserving the relative phase information of the signals on both analog inputs. The part accepts an analog input range of ±10 V (AD7863-10), ±2.5 V (AD7863-3) and 0 - 2.5 V (AD7863-2). Overvoltage protection on the analog inputs for the part allows the input voltage to go to ±17 V, ±7 V or +7 V respectively without causing damage.

A single conversion start signal ($\overline{CONVST}$) places both track/holds into hold simultaneously and initiates conversion on both channels. The BUSY signal indicates the end of conversion and at this time the conversion results for both channels are available to be read. The first read after a conversion accesses the result from V_{A1} or V_{B1}, while the second read accesses the result from V_{A2} or V_{B2}, depending on whether the multiplexer select A0 is low or high respectively. Data is read from the part via a 14-Bit parallel data bus with standard $\overline{CS}$ and $\overline{RD}$ signals.

FUNCTIONAL BLOCK DIAGRAM
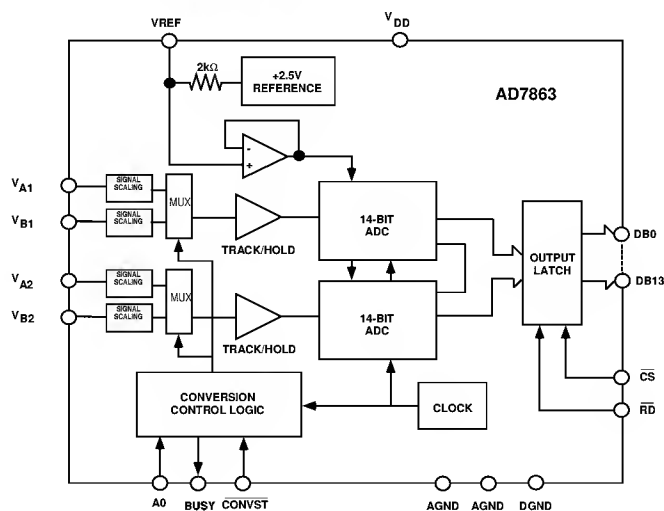
In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the part is also specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

The AD7863 is fabricated in Analog Devices' Linear Compatible CMOS (LC²MOS) process, a mixed technology process that combines precision bipolar circuits with low-power CMOS logic. It is available in 28-lead SSOP and SOIC.

PRODUCT HIGHLIGHTS

1. The AD7863 features two complete ADC functions allowing simultaneous sampling and conversion of two channels. Each ADC has a 2 channel input mux. The conversion result for both channels is available 4.5µs after initiating conversion.

2. The AD7863 operates from a single +5 V supply and consumes 75 mW typ. The automatic powerdown mode, where the part goes into power down once conversion is complete and "wakes up" before the next conversion cycle, makes the AD7863 ideal for battery-powered or portable applications.

3. The part offers a high speed parallel interface for easy connection to microprocessors, microcontrollers and digital signal processors.

4. The part is offered in three versions with different analog input ranges. The AD7863-10 offers the standard industrial input range of ±10V; the AD7863-3 offers the common signal processing input range of ±2.5V while the AD7863-2 can be used in unipolar 0 - +2.5V applications.

5. The part features very tight aperture delay matching between the two input sample & hold amplifiers.

Prelim A1 12/96

AD7863– SPECIFICATIONS

(V_{DD}= +5 V ±5%, AGND=DGND= 0V, REF = Internal.
All Specifications T_{MIN} to T_{MAX} unless otherwise noted).

Parameter	A Version[1]	B Version	Units	Test Conditions/Comments
SAMPLE AND HOLD				
-3dB Small Signal Bandwidth	3	3	MHz typ	
Aperture Delay	20	20	ns max	
Aperture Jitter	100	100	ps typ	
Aperture Delay Matching	200	200	ns max	
DYNAMIC PERFORMANCE[6]				f_{IN} = 100.0 kHz, f_S = 250 ksps
Signal to (Noise+Distortion) Ratio[3]				
@ 25°C	80	80	dB min	
Tmin to Tmax	78	80	dB min	
Total Harmonic Distortion[3]	-86	-90	dB max	
Peak Harmonic or Spurious Noise[3]	-86	-90	dB max	
Intermodulation Distortion[3]				fa = 49kHz, fb = 50kHz
2nd Order Terms	-86	-90	dB typ	
3rd Order Terms	-86	-90	dB typ	
Channel to Channel Isolation[3]	-86	-90	dB max	f_{IN} = 100kHz Sine Wave
DC ACCURACY				Any Channel
Resolution	14	14	Bits	
Minimum Resolution for which				
No Missing Codes are Guaranteed	14	14	Bits	
Relative Accuracy[3]	±2	±1	LSB max	
Differential Nonlinearity[3]	±1	±1	LSB max	
Positive Gain Error[3]	±4	±4	LSB max	
Positive Gain Error Match[3]	1	1	LSB max	
AD7863-10				
Negative Gain Error[3]	±4	±4	LSB max	
Bipolar Zero Error	±4	±4	LSB max	
Bipolar Zero Error Match	1	1	LSB max	
AD7863-3				
Negative Gain Error[3]	±4	±4	LSB max	
Bipolar Zero Error	±4	±4	LSB max	
Bipolar Zero Error Match	1	1	LSB max	
AD7863-2				
Unipolar Offset Error	+4	+4	LSB max	
Unipolar Offset Error Match	1	1	LSB max	
ANALOG INPUTS				
AD7863-10				
Input Voltage Range	±10	±10	Volts	Input
Input Resistance	9	9	kΩ typ	
AD7863-3				
Input Voltage Range	±2.5	±2.5	Volts	Input
Input Resistance	4	4	kΩ typ	
AD7863-2				
Input Voltage Range	+2.5	+2.5	Volts	Input
Input Current	500	500	nA max	
REFERENCE INPUT/OUTPUT				
REF IN Input Voltage Range	2.375/2.625	2.375/2.625		2.5V ± 5%
REF IN Input Impedance	1.6	1.6	kΩ min	Resistor Connected to Internal Reference Node.
REF IN Input Capacitance[4]	10	10	pF max	
REF OUT Output Voltage	2.5	2.5	V nom	
REF OUT Error @ 25°C	±10	±10	mV max	
REF OUT Error Tmin to Tmax	±20	±20	mV max	
REF OUT Temperature Coefficient	25	25	ppm/°C typ	
REF OUT Output Impedance	5	5	kΩ nom	See REF IN Input Impedance

AD7863- SPECIFICATIONS

(V_{DD} = +5 V ±5%, AGND=DGND= 0V, REF = Internal. All Specifications T_{MIN} to T_{MAX} unless otherwise noted).

Parameter Comments	A Version[1]	B Version		Units	Test Conditions/
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4		V min	V_{DD} = 5V±10%
Input Low Voltage, V_{INL}	0.8	0.8		V max	V_{DD} = 5V±10%
Input Current, I_{IN}	±10	±10		µA max	
Input Capacitance, C_{IN}[4]	10	10		pF max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	4.0	4.0		V min	I_{SOURCE} = 200µA
Output Low Voltage, V_{OL}	0.4	0.4		V max	I_{SINK} = 1.6mA
DB11 - DB0					
Floating-State Leakage Current	±10	±10		µA max	
Floating-State Capacitance[4]	10	10		pF max	
Output Coding					
AD7863-10, AD7863-3					Two's Complement
AD7863-2					Straight (Natural) Binary
CONVERSION RATE					
Conversion Time					
Mode 1 Operation	4.5	4.5		µs max	for both channels
Mode 2 Operation[5]	10	10		µs max	for both channels
Track/Hold Acquisition Time[2,3]	0.5	0.5		µs max	
POWER REQUIREMENTS					
V_{DD}	+5	+5		V nom	±10% for specified performance
I_{DD}					
Normal Mode (Mode 1)	15	15		mA max	
Power-Down Mode (Mode 2)					
I_{DD} @ 25°C	40	40		nA max	Logic Inputs = 0V or V_{DD}
T_{MIN} to T_{MAX}	200	200		nA max	Logic Inputs = 0V or V_{DD}
Power Dissipation					
Normal Mode	90	90		mW max	Typically 75 mW
Standby Mode @ 25°C	200	200		nW max	Typically 100 nW

NOTES
[1] Temperature Ranges are as follows : A, B Versions: -40°C to +85°C.
[2] Performance measured through full channel (multiplexer, SHA and ADC)
[3] See Terminology
[4] Sample tested @ 25°C to ensure compliance.
[5] This 10µs includes the "wake-up" time from standby. This "wake-up" time is timed from the rising edge of $\overline{CONVST}$, whereas conversion is timed from the falling edge of $\overline{CONVST}$, for a narrow $\overline{CONVST}$ pulse width the conversion time is effectively the "wake-up" time plus conversion time hence 10µs. This can be seen from Figure 6. Note that if the $\overline{CONVST}$ pulse width is greater than 6µs then the effective conversion time will increase beyond 10µs.
[6] Applies to mode 1 operation. See section on operating modes.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise noted)
V_{DD} to AGND..-0.3 V to +7 V
V_{DD} to DGND..-0.3 V to +7 V
Analog Input Voltage to AGND
   AD7863-10...±17 V
   AD7863-3...±7 V
   AD7863-2..+7 V
Reference Input Voltage to AGND...............-0.3V to V_{DD} +0.3 V
Digital Input Voltage to DGND......................-0.3V to V_{DD} +0.3V
Digital Output Voltage to DGND....................-0.3V to V_{DD} +0.3V
Operating Temperature Range
   Commercial (A, B Version)..........................-40°C to +85°C
   Extended (S Version)..................................-55°C to +125°C

Storage Temperature Range..........................-65°C to +150°C
Junction Temperature..+150°C
SOIC Package, Power Dissipation...............................450mW
  θ_{JA} Thermal Impedance..110°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec).................................. ....+215°C
    Infared (15 sec)..+220°C
SSOP Package, Power Dissipation...............................450mW
  θ_{JA} Thermal Impedance..110°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec)................................ ....+215°C
    Infared (15 sec)..+220°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TIMING CHARACTERISTICS[1,2] ($V_{D=}$= +5 V±5%, AGND=DGND= 0V, REF = Internal. All Specifications T_{MIN} to T_{MAX} unless otherwise noted).

Parameter	A, B Versions	S Version	Units	Test Conditions/Comments
t_{CONV}	4.5	4.5	μs max	Conversion Time
tacq	0.5	0.5	us max	Acquisition Time
Parallel Interface				
t_1	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_2	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_3	35	45	ns min	$\overline{CONVST}$ Pulse Width
t_4	35	45	ns min	Read Pulse Width
t_5[3]	25	35	ns min	Data Access Time After Falling Edge of $\overline{RD}$
	60	70	ns max	
t_6[4]	5	5	ns min	Bus Relinquish Time After Rising Edge of $\overline{RD}$
	30	40	ns max	
t7	40	40	ns min	Time between consecutive reads

NOTES

[1] Sample tested at 25°C to ensure compliance. All input signals are measured with tr = tf = 1ns (10% to 90% of +5V) and timed from a voltage level of +1.6 V.
[2] See Figure 1.
[3] Measured with the load circuit of Figure 2 and defined as the time required for an output to cross 0.8 V or 2.0 V.
[4] These times are derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

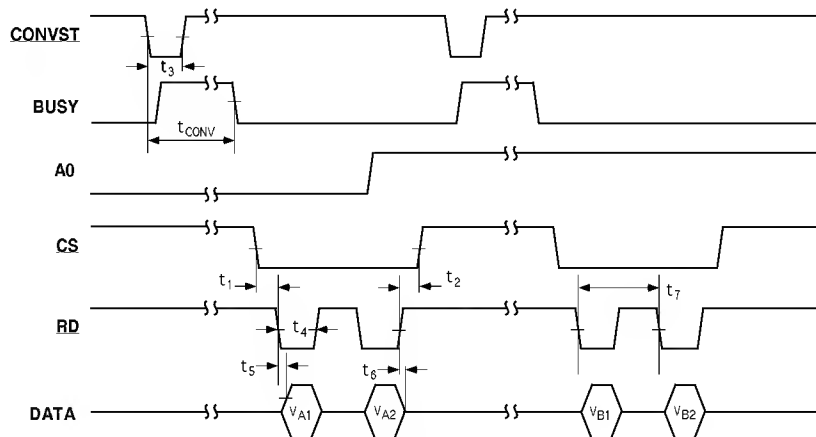Specifications subject to change without notice.
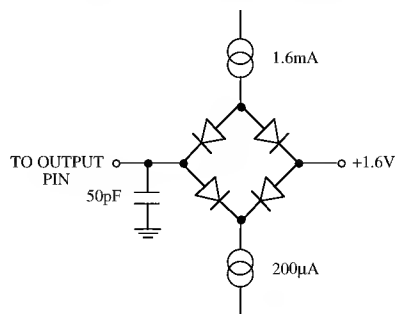

Figure 1. Timing Diagram

Figure 2. Load Circuit for Access Time and Bus Relinquish Time

ORDERING GUIDE

Model	Input Ranges	Relative Accuracy	Temperature Range	Package Option
AD7863AR-10	±10V	±1 LSB	-40°C to +85°C	R-28
AD7863BR-10	±10V	±0.5 LSB	-40°C to +85°C	R-28
AD7863ARS-10	±10V	±1 LSB	-40°C to +85°C	RS-28
AD7863AR-3	±2.5V	±1 LSB	-40°C to +85°C	R-28
AD7863BR-3	±2.5V	±0.5 LSB	-40°C to +85°C	R-28
AD7863ARS-3	±2.5V	±1 LSB	-40°C to +85°C	RS-28
AD7863AR-2	0V to 2.5V	±1 LSB	-40°C to +85°C	R-28
AD7863ARS-2	0V to 2.5V	±1 LSB	-40°C to +85°C	RS-28

*R=SOIC; RS = SSOP;

PIN CONFIGURATIONS
SOIC

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                 ┌───────  ───────┐
       DB12 │  1 │               │ 28 │ DB13
       DB11 │  2 │               │ 27 │ AGND
       DB10 │  3 │               │ 26 │ VB1
        DB9 │  4 │               │ 25 │ VA1
        DB8 │  5 │               │ 24 │ VDD
        DB7 │  6 │    AD7863     │ 23 │ BUSY
       DGND │  7 │   TOP VIEW    │ 22 │ RD
     CONVST │  8 │ (Not to Scale)│ 21 │ CS
        DB6 │  9 │               │ 20 │ A0
        DB5 │ 10 │               │ 19 │ VREF
        DB4 │ 11 │               │ 18 │ VA2
        DB3 │ 12 │               │ 17 │ VB2
        DB2 │ 13 │               │ 16 │ AGND
        DB1 │ 14 │               │ 15 │ DB0
                 └───────────────┘
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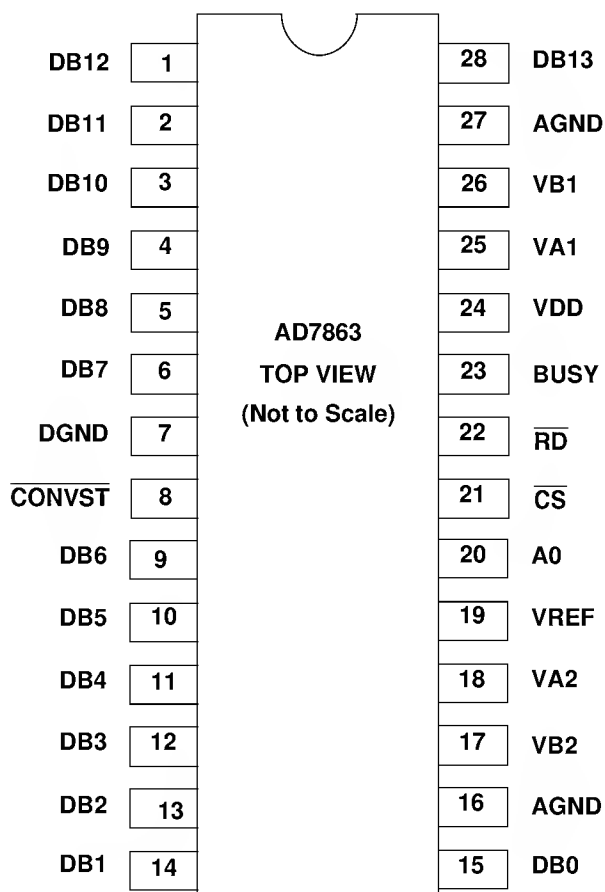
PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1 - 6	DB12- DB7	Data Bit 12 to Data Bit 7. Three-state TTL outputs.
7	DGND	Digital Ground. Ground reference for digital circuitry.
8	$\overline{\text{CONVST}}$	Convert Start Input. Logic Input. A high to low transition on this input puts both track/hold's into their hold mode and starts conversion on both channels.
9 - 15	DB6 - DB0	Data Bit 6 to Data Bit 0. Three-state TTL outputs.
16	AGND	Analog Ground. Ground reference for Mux, track/hold, reference and DAC circuitry.
17	V_{B2}	Input number 2 of channel B. Analog Input voltage range's of ± 10 V (AD7863-10), ± 2.5 V (AD7863-3) and 0 - 2.5 V (AD7863-2).
18	V_{A2}	Input number 2 of channel A. Analog Input voltage range's of ± 10 V (AD7863-10), ± 2.5 V (AD7863-3) and 0 - 2.5 V (AD7863-2).
19	VREF	Reference Input/Output. This pin is connected to the internal reference through a series resistor and is the output reference source for the analog-to-digital converter. The nominal reference voltage is 2.5 V and this appears at the pin.
20	A0	Multiplexer Select. This input is used in conjunction with RD and CS low to enable the data outputs. With A0 logic low, one read after a conversion will read the data from each of the ADC's in the sequence $V_{A1,}$ V_{A2} and a subsequent read, when A0 goes high, reads the data from $V_{B1,}$ V_{B2}.
21	$\overline{\text{CS}}$	Chip Select Input. Active low logic input. The device is selected when this input is active.
22	$\overline{\text{RD}}$	Read Input. Active low logic input. This input is used in conjunction with A0 and CS low to enable the data outputs. With A0 logic low, one read after a conversion will read the data from each of the ADC's in the sequence $V_{A1,}$ V_{A2} and a subsequent read, when A0 goes high, reads the data from $V_{B1,}$ V_{B2}.
23	BUSY	Busy Output. The busy output is triggered high by the falling edge of $\overline{\text{CONVST}}$ and remains high until conversion is completed.
24	VDD	Analog and Digital Positive Supply Voltage, +5.0 V $\pm 5\%$.
25	V_{A1}	Input number 1 of channel A. Analog Input voltage range's of ± 10 V (AD7863-10), ± 2.5 V (AD7863-3) and 0 - 2.5 V (AD7863-2).
26	V_{B1}	Input number 1 of channel B. Analog Input voltage range's of ± 10 V (AD7863-10), ± 2.5 V (AD7863-3) and 0 - 2.5 V (AD7863-2).
27	AGND	Analog Ground. Ground reference for Mux, track/hold, reference and DAC circuitry.
28	DB13	Data Bit 13 (MSB). Three-state TTL output. Output coding is 2's complement for the AD7863-10 and AD7863-3. Output coding is straight (natural) binary for the AD7863-2

TERMINOLOGY

Signal to (Noise + Distortion) Ratio

This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_s/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise +distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$\text{Signal to (Noise + Distortion)} = (6.02N + 1.76) \text{ dB}$$

Thus for a 14-Bit converter, this is 86.04 dB.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7863 it is defined as:

$$\text{THD(dB)} = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, and V_5 are the rms amplitudes of the second through the fifth harmonics.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_s/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m,n = 0,1,2,3, etc. Intermodulation terms are those for which neither m or n are equal to zero. For example, the second order terms include (fa + fb) and (fa - fb), while the third order terms include (2fa + fb), (2fa - fb), (fa + 2fb) and (fa - 2fb).

The AD7863 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dB's.

Channel to Channel Isolation

Channel to Channel isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale 100 kHz sine wave signal to each of the four inputs individually. These in turn are individually referenced to the other three channels whose inputs are grounded and the ADC output is measured to determine the level of crosstalk from the other channel. The figure given is the worst case across all four channels.

Relative Accuracy

Relative accuracy or endpoint nonlinearity is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Positive Full-Scale Error

This is the deviation of the last code transition (01.....110 to 01.....111) from the ideal 4 x VREF - 3/2 LSB (AD7863-10 ±10 V range) or VREF - 3/2 LSB (AD7863-3, ±2.5 V range), after the Bipolar Offset Error has been adjusted out.

Positive Full-Scale Error (AD7863-2, 0V to 2.5 V)

This is the deviation of the last code transition (01.....110 to 01.....111) from the ideal VREF - 3/2 LSB, after the unipolar offset error has been adjusted out.

Bipolar Zero Error (AD7863-10, ±10 V, AD7863-3, ±2.5 V)

This is the deviation of the mid-scale transition (all 1's to all 0's) from the ideal AGND - 1/2 LSB.

Unipolar Offset Error (AD7863-2, 0 V to 2.5 V)

This is the deviation of the first code transition (00.....000 to 00.....001) from the ideal AGND + 1/2 LSB.

Negative Full-Scale Error (AD7863-1, ±10 V, AD7863-3, ±2.5 V)

This is the deviation of the first code transition (10.....000 to 10.....001) from the ideal -4 x VREF + 1/2 LSB (AD7863-10 ±10 V range) or -VREF + 1/2 LSB (AD7863-3, ±2.5 V range), after Bipolar Zero Error has been adjusted out.

Track/Hold Acquisition Time

Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion (the point at which the track/hold returns to track mode). It also applies to situations where a change in the selected input channel takes place or where there is a step input change on the input voltage applied to the selected $V_{AX/BX}$ input of the AD7863. It means that the user must wait for the duration of the track/hold acquisition time after the end of conversion or after a channel change/step input change to $V_{AX/BX}$ before starting another conversion, to ensure that the part operates to specification.

CONVERTER DETAILS

The AD7863 is a high speed, low power, dual 14-Bit A/D converter that operates from a single +5 V supply. The part contains two 4.5 μs successive approximation ADCs, two track/hold amplifiers, an internal +2.5 V reference and a high speed parallel interface. There are 4 analog inputs which are grouped into two channels (A & B) selected by the A0 input. Each channel has two inputs (V_{A1} & V_{A2} or V_{B1} & $V_{B2)}$ which can be sampled and converted simultaneously thus preserving the relative phase information of the signals on both analog inputs. The part accepts an analog input range of ± 10 V (AD7863-10), ± 2.5 V (AD7863-3) and 0 - 2.5 V (AD7863-2). Overvoltage protection on the analog inputs for the part allows the input voltage to go to ± 17 V, ± 7 V or +7 V respectively without causing damage. The AD7863 has two operating modes, the high sampling mode and the auto sleep mode where the part automatically goes into sleep after the end of conversion. These modes are discussed in more detail in the Timing and Control Section.

Conversion is initiated on the AD7863 by pulsing the $\overline{CONVST}$ input. On the falling edge of $\overline{CONVST}$, both on-chip track/holds are placed into hold simultaneously and the conversion sequence is started on both channels. The conversion clock for the part is generated internally using a laser-trimmed clock oscillator circuit. The $\overline{BUSY}$ signal indicates the end of conversion and at this time the conversion results for both channels are available to be read. The first read after a conversion accesses the result from V_{A1} or V_{B1} while the second read accesses the result from V_{A2} or V_{B2} depending on whether the multiplexer select A0 is low or high respectively. Data is read from the part via a 14-Bit parallel data bus with standard $\overline{CS}$ and $\overline{RD}$ signals.

Conversion time for the AD7863 is 4.5 μs in the high sampling mode (10 us for the auto sleep mode), and the track/hold acquisition time is 0.5 μs. To obtain optimum performance from the part, the read operation should not occur during the conversion or during 500 ns prior to the next conversion. This allows the part to operate at throughput rates up to 200 kHz and achieve data sheet specifications.

Track/Hold Section

The track/hold amplifiers on the AD7863 allows the ADC's to accurately convert an input sine wave of full-scale amplitude to 14-Bit accuracy. The input bandwidth of the track/hold is greater than the Nyquist rate of the ADC even when the ADC is operated at its maximum throughput rate of 200 kHz (i.e., the track/hold can handle input frequencies in excess of 100 kHz).

The track/hold amplifiers acquire input signals to 14-Bit accuracy in less than 500 ns. The operation of the track/holds are essentially transparent to the user. The two track/hold amplifiers sample their respective input channels simultaneously, on the falling edge of $\overline{CONVST}$. The aperture time for the track/holds (i.e., the delay time between the external $\overline{CONVST}$ signal and the track/hold actually going into hold) are typically 15 ns and, more importantly, is well matched across the two track/holds on one device and also well matched from device to device. This allows the relative phase information between different input channels to be accurately preserved. It also allows multiple AD7863s to sample more than two chan-

nels simultaneously. At the end of conversion, the part returns to its tracking mode. The acquisition time of the track/hold amplifiers begin at this point.

Reference Section

The AD7863 contains a single reference pin, labelled VREF, which either provides access to the part's own +2.5 V reference or to which an external +2.5 V reference can be connected to provide the reference source for the part. The part is specified with a +2.5 V reference voltage. Errors in the reference source will result in gain errors in the AD7863's transfer function and will add to the specified full-scale errors on the part. On the AD7863-10 and AD7863-3, it will also result in an offset error injected in the attenuator stage.

The AD7863 contains an on-chip +2.5 V reference. To use this reference as the reference source for the AD7863, simply connect a 0.2 μF disc ceramic capacitor from the VREF pin to AGND. The voltage that appears at this pin is internally buffered before being applied to the ADC. If this reference is required for use external to the AD7863, it should be buffered as the part has a FET switch in series with the reference output resulting in a source impedance for this output of 5.5 kΩ nominal. The tolerance on the internal reference is ± 10 mV at 25°C with a typical temperature coefficient of 25 ppm/°C and a maximum error over temperature of ± 25 mV.

If the application requires a reference with a tighter tolerance or the AD7863 needs to be used with a system reference, then the user has the option of connecting an external reference to this VREF pin. The external reference will effectively overdrive the internal reference and thus provide the reference source for the ADC. The reference input is buffered before being applied to the ADC with the maximum input current is ± 100 μA. Suitable reference sources for the AD7863 include the AD680 and AD780 precision +2.5 V references.

CIRCUIT DESCRIPTION

Analog Input Section

The AD7863 is offered as three part types, the AD7863-10 which handles a ± 10 V input voltage range, the AD7863-3 which handles input voltage range ± 2.5 V and the AD7863-2 which handles a 0 V to +2.5 V input voltage range.
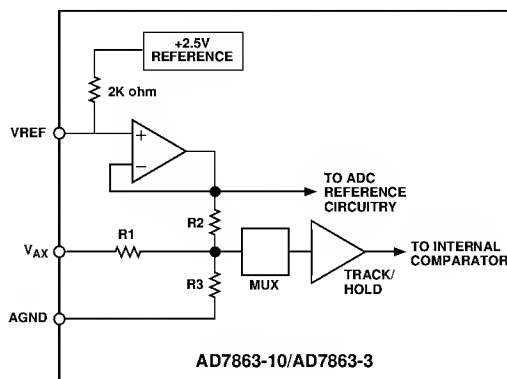

Figure 3. AD7863-10/-3 Analog Input Structure

Figure 3 shows the analog input section for the AD7863-10 and AD7863-3. The analog input range of the AD7863-10 is ±10 V into an input resistance of typically 9 kΩ. The analog input range of the AD7863-3 is ±2.5 V into an input resistance of typically 4 kΩ. This input is benign with no dynamic charging currents as the resistor stage is followed by a high input impedance stage of the track/hold amplifier. For the AD7863-10, R1 = 8 kΩ, R2 = 2 kΩ and R3 = 2k6 Ω. For the AD7863-3, R1 = R2 = 2 kΩ and R3 is open circuit.

For the AD7863-10 and AD7863-3, the designed code transitions occur on successive integer LSB values (i.e., 1 LSB, 2 LSBs, 3 LSBs . . .). Output coding is 2s complement binary with 1 LSB = FS/16384. The ideal input/output transfer function for the AD7863-10 and AD7863-3 is shown in Table I.

TABLE I. IDEAL INPUT/OUTPUT CODE TABLE FOR THE AD7863-10/-3

Analog Input[1]	Digital Output Code Transition
+FSR/2 – 1 LSB[2]	011 . . . 110 to 011 . . . 111
+FSR/2 – 2 LSBs	011 . . . 101 to 011 . . . 110
+FSR/2 – 3 LSBs	011 . . . 100 to 011 . . . 101
GND + 1 LSB	000 . . . 000 to 000 . . . 001
GND	111 . . . 111 to 000 . . . 000
GND – 1 LSB	111 . . . 110 to 111 . . . 111
–FSR/2 + 3 LSBs	100 . . . 010 to 100 . . . 011
–FSR/2 + 2 LSBs	100 . . . 001 to 100 . . . 010
–FSR/2 + 1 LSB	100 . . . 000 to 100 . . . 001

NOTES
[1]FSR is full-scale range = 20 V (AD7863-10) and = 5V (AD7863-3) with REF IN = +2.5 V.
[2]1 LSB = FSR/16384 = 1.22 mV (AD7863-10) and 0.3 mV (AD7863-3) with REF IN = +2.5 V.

The analog input section for the AD7863-2 contains no biasing resistors and the $V_{AX/BX}$ pin drives the input to the multiplexer and track/hold amplifier circuitry directly. The analog input range is 0 V to +2.5 V into a high impedance stage with an input current of less than 500 nA. This input is benign with no dynamic charging currents. Once again, the designed code transitions occur on successive integer LSB values. Output coding is straight (natural) binary with 1 LSB = FS/16384 = 2.5 V/16384 = 0.15 mV. Table II shows the ideal input/output transfer function for the AD7863-2.

TABLE II. IDEAL INPUT/OUTPUT CODE TABLE FOR THE AD7863-2

Analog Input[1]	Digital Output Code Transition
+FSR – 1 LSB[2]	111 . . . 110 to 111 . . . 111
+FSR – 2 LSB	111 . . . 101 to 111 . . . 110
+FSR – 3 LSB	111 . . . 100 to 111 . . . 101
GND + 3 LSB	000 . . . 010 to 000 . . . 011
GND + 2 LSB	000 . . . 001 to 000 . . . 010
GND + 1 LSB	000 . . . 000 to 000 . . . 001

NOTES
[1]FSR is Full-Scale Range and is 2.5 V for AD7863-2 with VREF = +2.5 V.
[2]1 LSB = FSR/16384 and is 0.15 mV for AD7863-2 with VREF = +2.5 V.

OFFSET AND FULL-SCALE ADJUSTMENT

In most Digital Signal Processing (DSP) applications, offset and full-scale errors have little or no effect on system performance. Offset error can always be eliminated in the analog domain by ac coupling. Full-scale error effect is linear and does not cause problems as long as the input signal is within the full dynamic range of the ADC. Invariably, some applications will require that the input signal span the full analog input dynamic range. In such applications, offset and full-scale error will have to be adjusted to zero.

Figure 4 shows a circuit which can be used to adjust the offset and full-scale errors on the AD7863 (V_{A1} on the AD7863-10 version is shown for example purposes only). Where adjustment is required, offset error must be adjusted before full-scale error. This is achieved by trimming the offset of the op amp driving the analog input of the AD7863 while the input voltage is a 1/2 LSB below analog ground. The trim procedure is as follows: apply a voltage of –0.61 mV (–1/2 LSB) at V_{A1} in Figure 4 and adjust the op amp offset voltage until the ADC output code flickers between 1111 1111 1111 and 0000 0000 0000.
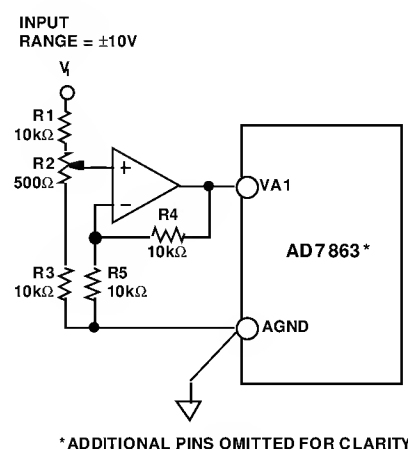

Figure 4. AD7863 Full-Scale Adjust Circuit

Gain error can be adjusted at either the first code transition (ADC negative full scale) or the last code transition (ADC positive full scale). The trim procedures for both cases are as follows:

Positive Full-Scale Adjust

Apply a voltage of +9.9927 V (FS/2 – 3/2 LSBs) at V_{A1}. Adjust R2 until the ADC output code flickers between 0111 1111 1110 and 0111 1111 1111.

Negative Full-Scale Adjust

Apply a voltage of –9.9976 V (–FS + 1/2 LSB) at V_{A1} and adjust R2 until the ADC output code flickers between 1000 0000 0000 and 1000 0000 0001.

An alternative scheme for adjusting full-scale error in systems which use an external reference is to adjust the voltage at the VREF pin until the full-scale error for any of the channels is adjusted out. The good full-scale matching of the channels will ensure small full-scale errors on the other channels.

TIMING AND CONTROL

Figure 5(a) shows the timing and control sequence required to obtain optimum performance (Mode 1) from the AD7863. In the sequence shown, a conversion is initiated on the falling edge of $\overline{\text{CONVST}}$. This places both track/holds into hold simultaneously and new data from this conversion is available in the output register of the AD7863 4.5 µs later. The BUSY signal indicates the end of conversion and at this time the conversion results for both channels are available to be read. A second conversion is then initiated. If the multiplexer select A0 is low, the first and second read pulses after the first conversion accesses the result from channel A (V_{A1} and V_{A2} respectively). The third and fourth read pulses, after the second conversion and A0 high, accesses the result from channel B (V_{B1} and V_{B2} respectively). A0's state can be changed any time after the $\overline{\text{CONVST}}$ goes high, i.e., track/holds into hold, and 500ns prior to the next falling edge of $\overline{\text{CONVST}}$. Data is read from the part via a 14-Bit parallel data bus with standard $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signal, i.e., the read operation consists of a negative going pulse on the $\overline{\text{CS}}$ pin combined with two negative going pulses on the $\overline{\text{RD}}$ pin (while the $\overline{\text{CS}}$ is low), accessing the two 14-Bit results. Once the read operation has taken place, a further 500 ns should be allowed before the next falling edge of $\overline{\text{CONVST}}$ to optimize the settling of the track/hold amplifier before the next conversion is initiated. With the internal clock frequency at its maximum (XX MHz - not accessible externally), the achievable throughput rate for the part is 4.5 µs (conversion time) plus 200ns (read time) plus 0.5 µs (acquisition time). This results in a minimum throughput time of 5.2 µs (equivalent to a throughput rate of 192 kHz).

Read Options

Apart from the Read Operation described above and displayed in Figure 5(a), other $\overline{\text{CS}}$ and $\overline{\text{RD}}$ combinations can result in different channels/inputs being read in different combinations. Suitable combinations are shown in Figure 5(b) through 5(d).
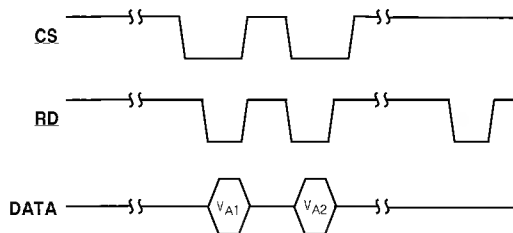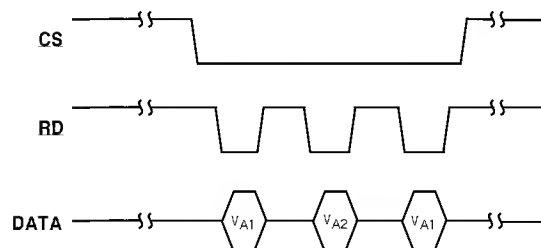

Figure 5(b). Read Option A
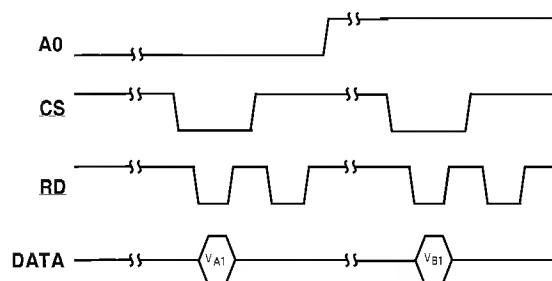

Figure 5(c). Read Option B
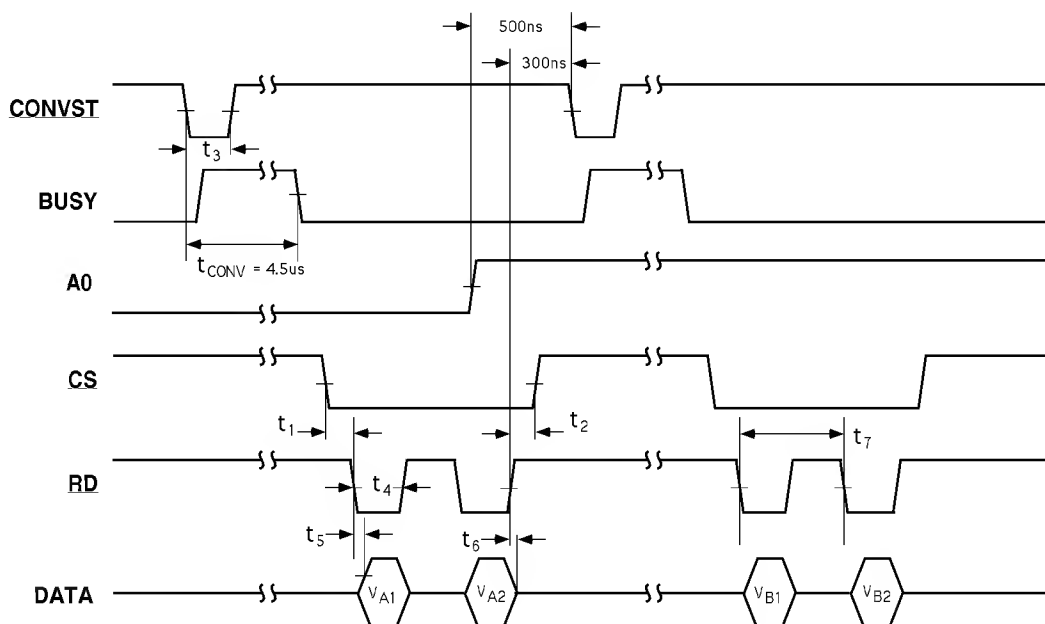

Figure 5(d). Read Option C

Figure 5(a). Mode 1 Timing Operation Diagram for High Sampling Performance

*   When using an EXTERNAL REFERENCE, WAKE-UP TIME = 2.5μs.
**   When using an INTERNAL REFERENCE, WAKE-UP TIME = 5ms.
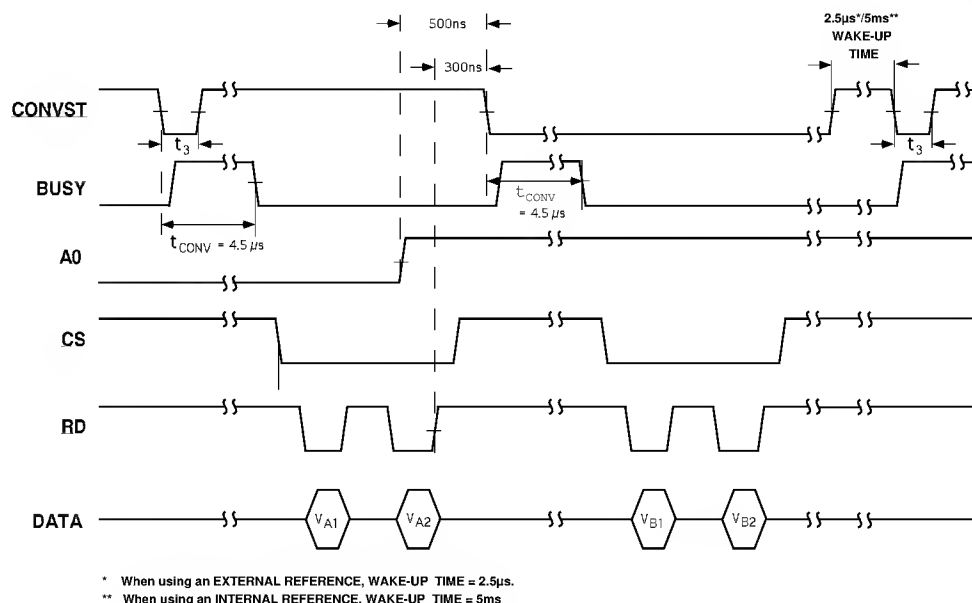
Figure 6. AD7863 Mode 2 Timing Diagram Where Automatic Sleep function is Initiated

OPERATING MODES

Mode 1 Operation (High Sampling Performance)

The timing diagram in Figure 5(a) is for optimum performance in operating mode 1 where the falling edge of $\overline{CONVST}$ starts conversion and puts the Track/Hold amplifier's into their hold mode. This falling edge of $\overline{CONVST}$ also causes the BUSY signal to go high to indicate that a conversion is taking place. The BUSY signal goes low when the conversion is complete which is 4.5μs max after the falling edge of $\overline{CONVST}$ and new data from this conversion is available in the output latch of the AD7863. A read operation accesses this data. If the multiplexer select A0 is low, the first and second read pulses after the first conversion accesses the result from channel A (V_{A1} and V_{A2} respectively). The third and fourth read pulses, after the second conversion and A0 high, accesses the result from channel B (V_{B1} and V_{B2} respectively). Data is read from the part via a 14-Bit parallel data bus with standard $\overline{CS}$ and $\overline{RD}$ signals. This data read operation consists of negative going pulse on the $\overline{CS}$ pin combined with two negative going pulses on the $\overline{RD}$ pin (while the $\overline{CS}$ is low) , accessing the two 14-Bit results. For the fastest throughput rate (with an internal clock of XX MHz) the read operation will take 200 ns. The read operation must be complete at least 500 ns before the falling edge of the next $\overline{CONVST}$ and this gives a total time of 5.2 μs for the full throughput time (equivalent to 192 kHz). This mode of operation should be used for high sampling applications.

Mode 2 Operation (Auto Sleep After Conversion)

The timing diagram in Figure 6 is for optimum performance in operating mode 2 where the part automatically goes into sleep mode once BUSY goes low after conversion and "wakes-up" before the next conversion takes place. This is achieved by keeping $\overline{CONVST}$ low at the end of the second conversion whereas it was high at the end of the second conversion for

mode 1 operation. The operation shown in figure 6 shows how to access data from both channels A and B followed by the Auto Sleep mode. One can also setup the timing to access data from channel A only or channel B only (see Read Options section on previous page) and then go into Auto-Sleep mode. The rising edge of $\overline{CONVST}$ "wakes-up" the part. This wake-up time is 2.5 μs when using an external reference and 5ms when using the internal reference at which point the Track/Hold amplifier's go into their hold mode provided the $\overline{CONVST}$ has gone low. The conversion takes 4.5μs after this giving a total of 7 μs (external reference, 5.0035ms for internal reference) from the rising edge of $\overline{CONVST}$ to the conversion being complete which is indicated by the BUSY going low. Note that since the wake-up time from the rising edge of $\overline{CONVST}$ is 2.5μs, if the $\overline{CONVST}$ pulse width is greater than 2.5μs the conversion will take more than the 7μs (2.5μs wake-up time + 4.5μs conversion time) shown in diagram from the rising edge of $\overline{CONVST}$. This is because the Track/Hold amplifiers go into their hold mode on the falling edge of $\overline{CONVST}$ and then the conversion will not be complete for a further 4.5μs. In this case the BUSY will be the best indicator for when the conversion is complete. Even though the part is in sleep mode data can still be read from the part. The read operation is identical to that in as in mode 1 operation, and must also be complete at least 500 ns before the falling edge of the next $\overline{CONVST}$ to allow the Track/Hold amplifier's to have enough time to settle. This mode is very useful when the part is converting at a slow rate as the power consumption will be significantly reduced from that of mode 1 operation.

AD7863 DYNAMIC SPECIFICATIONS

The AD7863 is specified and 100% tested for dynamic performance specifications as well as traditional dc specifications such as Integral and Differential Nonlinearity. These ac specifications are required for the signal processing applications such as phased array sonar, adaptive filters and spectrum analysis. These applications require information on the ADC's effect on

the spectral content of the input signal. Hence, the parameters for which the AD7863 is specified include SNR, harmonic distortion, intermodulation distortion and peak harmonics. These terms are discussed in more detail in the following sections.

Signal-to-Noise Ratio (SNR)
SNR is the measured signal to noise ratio at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency (fs/2) excluding dc. SNR is dependent upon the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to noise ratio for a sine wave input is given by

$$SNR = (6.02N + 1.76) \text{ dB} \qquad (1)$$

where N is the number of bits.

Thus for an ideal 14-bit converter, SNR = 86.04 dB.

Figure 7 shows a histogram plot for 8192 conversions of a dc input using the AD7863 with 5 V supply. The analog input was set at the center of a code transition. It can be seen that all the codes appear in the one output bin indicating very good noise performance from the ADC.

Figure 7. Histogram of 8192 Conversions of a DC Input

The same data is presented in Figure 8 as in Figure 7 except that in this case the output data read for the device occurs during conversion. This has the effect of injecting noise onto the die while bit decisions are being made and this increases the noise generated by the AD7863. The histogram plot for 8192 conversions of the same dc input now shows a larger spread of codes. This effect will vary depending on where the serial clock edges appear with respect to the bit trials of the conversion process. It is possible to achieve the same level of performance when reading during conversion as when reading after conversion depending on the relationship of the serial clock edges to the bit trial points.

The output spectrum from the ADC is evaluated by applying a sine wave signal of very low distortion to the $V_{AX/BX}$ input which is sampled at a XXX kHz sampling rate. A Fast Fourier Transform (FFT) plot is generated from which the SNR data can be obtained. Figure 7 shows a typical 2048 point FFT plot of the AD7863 with an input signal of 10 kHz and a sampling frequency of XXX kHz. The SNR obtained from this graph is XX.XX dB. It should be noted that the harmonics are taken into account when calculating the SNR.

Figure 8. Histogram of 8192 Conversions with Read During Conversion

Figure 9. AD7863 FFT Plot

Effective Number of Bits
The formula given in Equation 1 relates the SNR to the number of bits. Rewriting the formula, as in Equation 2, it is possible to get a measure of performance expressed in effective number of bits (N).

$$N = \frac{SNR - 1.76}{6.02} \qquad (2)$$

The effective number of bits for a device can be calculated directly from its measured SNR.

Figure 10 shows a typical plot of effective number of bits versus frequency for an AD7863-2 with a sampling frequency of XXX kHz. The effective number of bits typically falls between XX.X and XX.X corresponding to SNR figures of XX.XX dB and XX.XX dB.

Figure 10. Effective Numbers of Bits vs. Frequency

Total Harmonic Distortion (THD)

Total Harmonic Distortion (THD) is the ratio of the rms sum of harmonics to the rms value of the fundamental. For the AD7863, THD is defined as

$$THD(dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4 and V_5 are the rms amplitudes of the second through the sixth harmonic. The THD is also derived from the FFT plot of the ADC output spectrum.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of $mfa \pm nfb$ where m, n = 0, 1, 2, 3 . . ., etc. Intermodulation terms are those for which neither m or n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb) while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

Using the CCIF standard where two input frequencies near the top end of the input bandwidth are used, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs. In this case, the input consists of two, equal amplitude, low distortion sine waves. Figure 11 shows a typical IMD plot for the AD7863.

Figure 12. This shows very good integral linearity performance from the AD7863 at an input frequency of 10 kHz. The absence of large spikes in the plot shows good differential linearity. Simplified versions of the formulae used are outlined below.

$$INL(i) = \left[\frac{(V(i) - V(o)) \cdot 4096}{V(fs) - V(o)} \right] - i$$

where $INL(i)$ is the integral linearity at code i. V(fs) and V(o) are the estimated full-scale and offset transitions, and V(i) is the estimated transition for the ith code.

V(i), the estimated code transition point is derived as follows:

$$V(i) = -A \cdot Cos \frac{\left[\pi \cdot cum(i) \right]}{N}$$

where A is the peak signal amplitude, N is the number of histogram samples

$$and \; cum(i) = \sum_{n=o}^{i} V(n) occurrences$$

Figure 12.. AD7863 AC INL Plot

Power Considerations

In the automatic power-down mode then the part may be operated at a sample rate which is considerably less than 200 kHz. In this case the power consumption will be reduced and will depend on the sample rate. Figure 13 shows a graph of the power consumption versus sampling rates from 10 Hz to 1 kHz in the automatic power-down mode. The conditions are 5 V supply 25°C and the data was read after conversion.

Figure 11. AD7863 IMD Plot

Peak Harmonic or Spurious Noise

Harmonic or Spurious Noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to fs/2 and excluding dc) to the rms value of the fundamental. Normally, the value of this specification will be determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor the peak will be a noise peak.

AC Linearity Plot

When a sine wave of specified frequency is applied to the V_{IN} input of the AD7863 and several million samples are taken, a histogram showing the frequency of occurrence of each of the 4096 ADC codes can be generated. From this histogram data it is possible to generate an ac integral linearity plot as shown in

Figure 13. *Power vs. Sample Rate in Auto Power-Down Mode*

MICROPROCESSOR INTERFACING

The AD7863 high speed bus timing allows direct interfacing to DSP processors as well as modern 16-bit microprocessors. Suitable microprocessor interfaces are shown in Figures 14 through 18.

AD7863–ADSP-2100 Interface

Figure 14 shows an interface between the AD7863 and the ADSP-2100. The $\overline{\text{CONVST}}$ signal can be supplied from the ADSP-2100 or from an external source. The AD7863 BUSY line provides an interrupt to the ADSP-2100 when conversion is completed on all four channels. The four conversion results can then be read from the AD7863 using four successive reads to the same memory address. The following instruction reads one of the four results (this instruction is repeated four times to read all four results in sequence):

$$MR0 = DM(ADC)$$

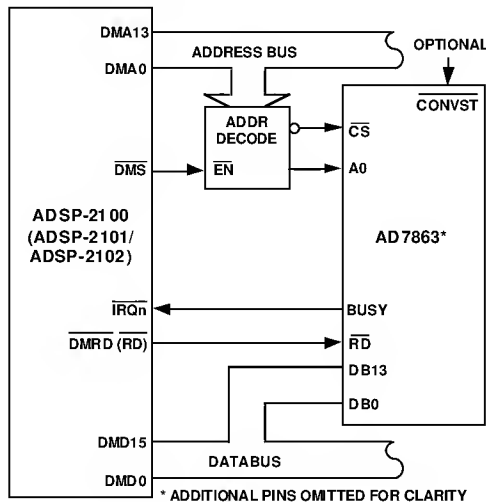where MR0 is the ADSP-2100 MR0 register and ADC is the AD7863 address.

Figure 14. *AD7863–ADSP-2100 Interface*

AD7863–ADSP-2101/ADSP-2102 Interface

The interface outlined in Figure 14 also forms the basis for an interface between the AD7863 and the ADSP-2101/ADSP-2102. The READ line of the ADSP-2101/ADSP-2102 is labeled $\overline{\text{RD}}$. In this interface, the $\overline{\text{RD}}$ pulse width of the processor can be programmed using the Data Memory Wait State Control Register. The instruction used to read one of the four results is as outlined for the ADSP-2100.
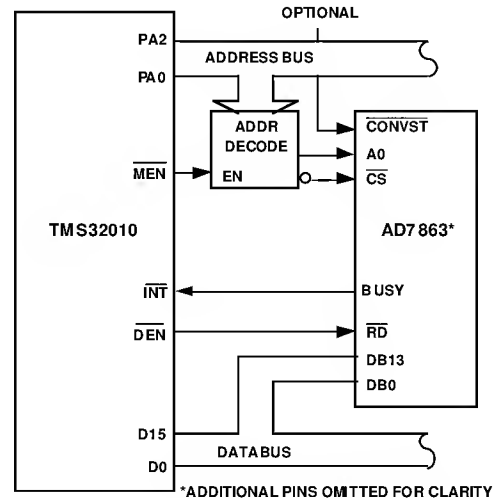

Figure 15. *AD7863–TMS32010 Interface*

AD7863–TMS32010 Interface

An interface between the AD7863 and the TMS32010 is shown in Figure 15. Once again the $\overline{\text{CONVST}}$ signal can be supplied from the TMS32010 or from an external source and the TMS32010 is interrupted when both conversions have been completed. The following instruction is used to read the conversion results from the AD7863:

$$IN\ D,ADC$$

where D is Data Memory address and ADC is the AD7863 address.

AD7863–TMS320C25 Interface

Figure 16 shows an interface between the AD7863 and the TMS320C25. As with the two previous interfaces, conversion can be initiated from the TMS320C25 or from an external source and the processor is interrupted when the conversion sequence is completed. The TMS320C25 does not have a separate $\overline{\text{RD}}$ output to drive the AD7863 $\overline{\text{RD}}$ input directly. This has to be generated from the processor STRB and R/$\overline{\text{W}}$ outputs with the addition of some logic gates. The $\overline{\text{RD}}$ signal is OR-gated with the MSC signal to provide the one WAIT state required in the read cycle for correct interface timing. Conversion results are read from the AD7863 using the following instruction:

$$IN\ D,ADC$$

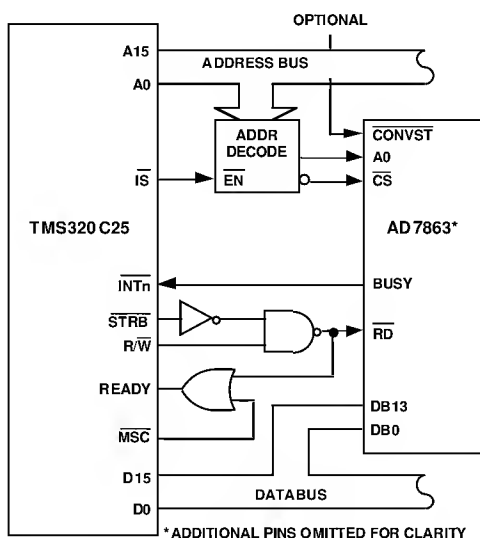where D is Data Memory address and ADC is the AD7863 address.

Figure 16. AD7863–TMS320C25 Interface

Some applications may require that the conversion is initiated by the microprocessor rather than an external timer. One option is to decode the AD7863 $\overline{\text{CONVST}}$ from the address bus so that a write operation starts a conversion. Data is read at the end of the conversion sequence as before. Figure 18 shows an example of initiating conversion using this method. Note that for all interfaces, it is preferred that a read operation should not be attempted during conversion.

AD7863–MC68000 Interface
An interface between the AD7863 and the MC68000 is shown in Figure 17. As before, conversion can be supplied from the MC68000 or from an external source. The AD7863 BUSY line can be used to interrupt the processor or, alternatively, software delays can ensure that conversion has been completed before a read to the AD7863 is attempted. Because of the nature of its interrupts, the 68000 requires additional logic (not shown in Figure 18) to allow it to be interrupted correctly. For further information on 68000 interrupts, consult the 68000 users manual.

The MC68000 $\overline{\text{AS}}$ and R/$\overline{\text{W}}$ outputs are used to generate a separate $\overline{\text{RD}}$ input signal for the AD7863. $\overline{\text{CS}}$ is used to drive the 68000 $\overline{\text{DTACK}}$ input to allow the processor to execute a normal read operation to the AD7863. The conversion results are read using the following 68000 instruction:

MOVE.W ADC,D0

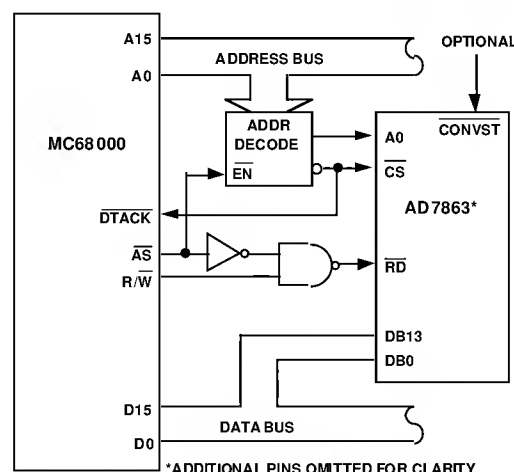where D0 is the 68000 D0 register and ADC is the AD7863 address.

Figure 17. AD7863–MC68000 Interface

AD7863–80C196 Interface
Figure 18 shows an interface between the AD7863 and the 80C196 microprocessor. Here, the microprocessor initiates conversion. This is achieved by gating the 80C196 $\overline{\text{WR}}$ signal with a decoded address output (different to the AD7863 $\overline{\text{CS}}$ address). The AD7863 BUSY line is used to interrupt the microprocessor when the conversion sequence is completed.
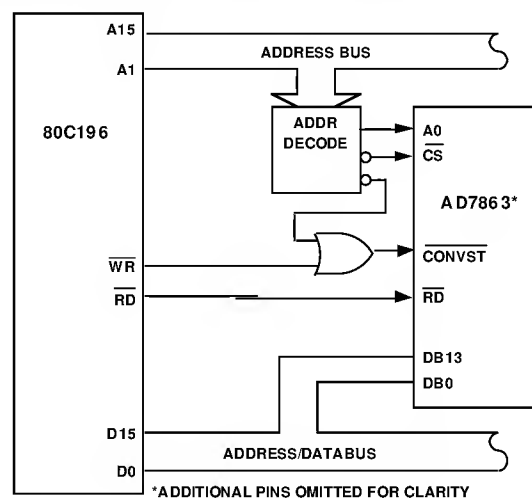

Figure 18. AD7863–80C196 Interface

Vector Motor Control
The current drawn by a motor can be split into two components: one produces torque and the other produces magnetic flux. For optimal performance of the motor, these two components should be controlled independently. In conventional methods of controlling a three-phase motor, the current (or voltage) supplied to the motor and the frequency of the drive are the basic control variables. However, both the torque and flux are functions of current (or voltage) and frequency. This coupling effect can reduce the performance of the motor because, for example, if the torque is increased by increasing the frequency, the flux tends to decrease.

Vector control of an ac motor involves controlling phase in addition to drive and current frequency. Controlling the phase of the motor requires feedback information on the position of the rotor relative to the rotating magnetic field in the motor. Using this information, a vector controller mathematically

AD7863

transforms the three phase drive currents into separate torque and flux components. The AD7863, with its four-channel simultaneous sampling capability, is ideally suited for use in vector motor control applications.

A block diagram of a vector motor control application using the AD7863 is shown in Figure 19. The position of the field is derived by determining the current in each phase of the motor. Only two phase currents need to be measured because the third can be calculated if two phases are known. V_{A1} and V_{A2} of the AD7863 are used to digitize this information.

Simultaneous sampling is critical to maintain the relative phase information between the two channels. A current sensing isolation amplifier, transformer or Hall effect sensor is used between the motor and the AD7863. Rotor information is obtained by measuring the voltage from two of the inputs to the motor. V_{B1} and V_{B2} of the AD7863 are used to obtain this information. Once again the relative phase of the two channels is important. A DSP microprocessor is used to perform the mathematical transformations and control loop calculations on the information fed back by the AD7863.
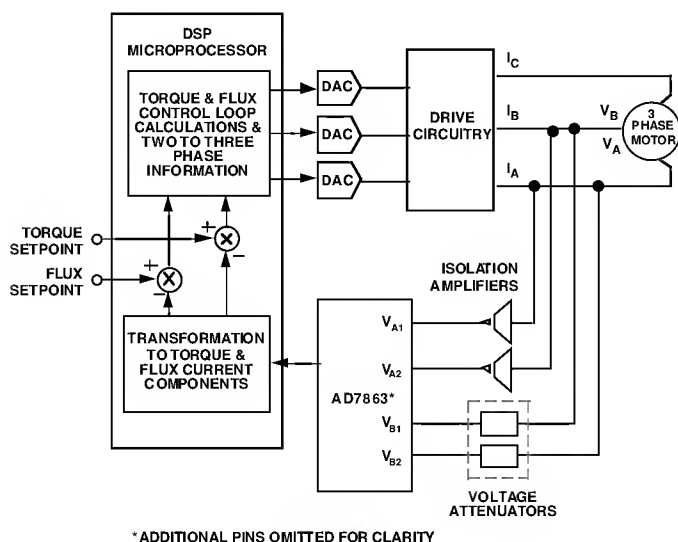
external or system reference can be used to drive all VREF inputs. A common reference ensures good full-scale tracking between all channels.

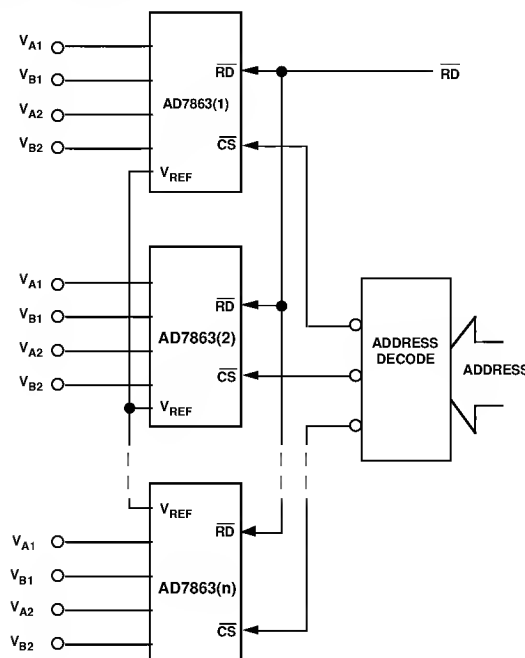*Figure 20. Multiple AD7863s in Multichannel System*

Figure 19. Vector Motor Control Using the AD7863.

MULTIPLE AD7863S

Figure 20 shows a system where a number of AD7863s can be configured to handle multiple input channels. This type of configuration is common in applications such as sonar, radar, etc. The AD7863 is specified with typical limits on aperture delay. This means that the user knows the difference in the sampling instant between all channels. This allows the user to maintain relative phase information between the different channels.

A common read signal from the microprocessor drives the $\overline{RD}$ input of all AD7863s. Each AD7863 is designated a unique address selected by the address decoder. The reference output of AD7863 number 1 is used to drive the reference input of all other AD7863s in the circuit shown in Figure 20. One VREF pin can drive several AD7863 REF IN pins. Alternatively, an

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).